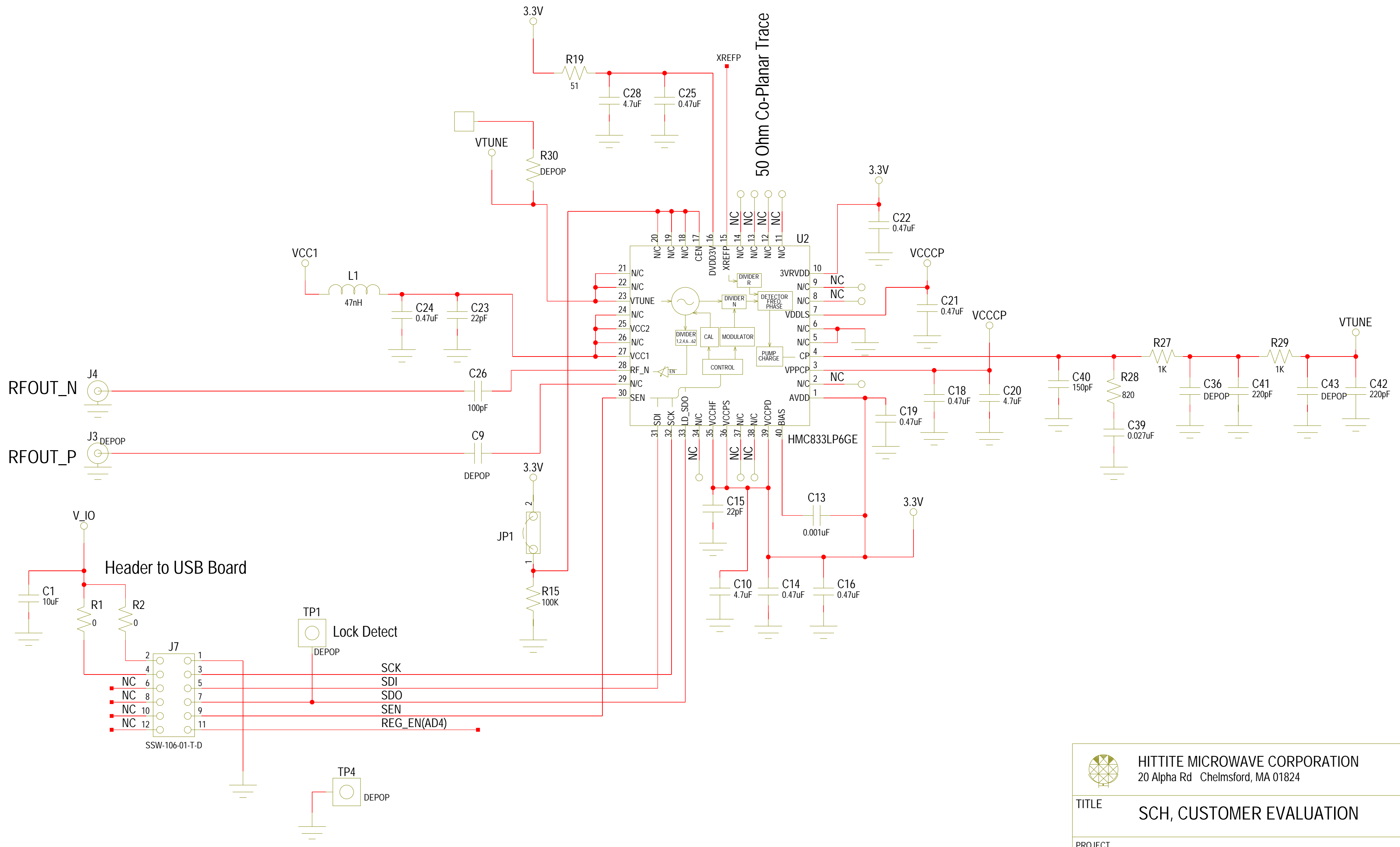

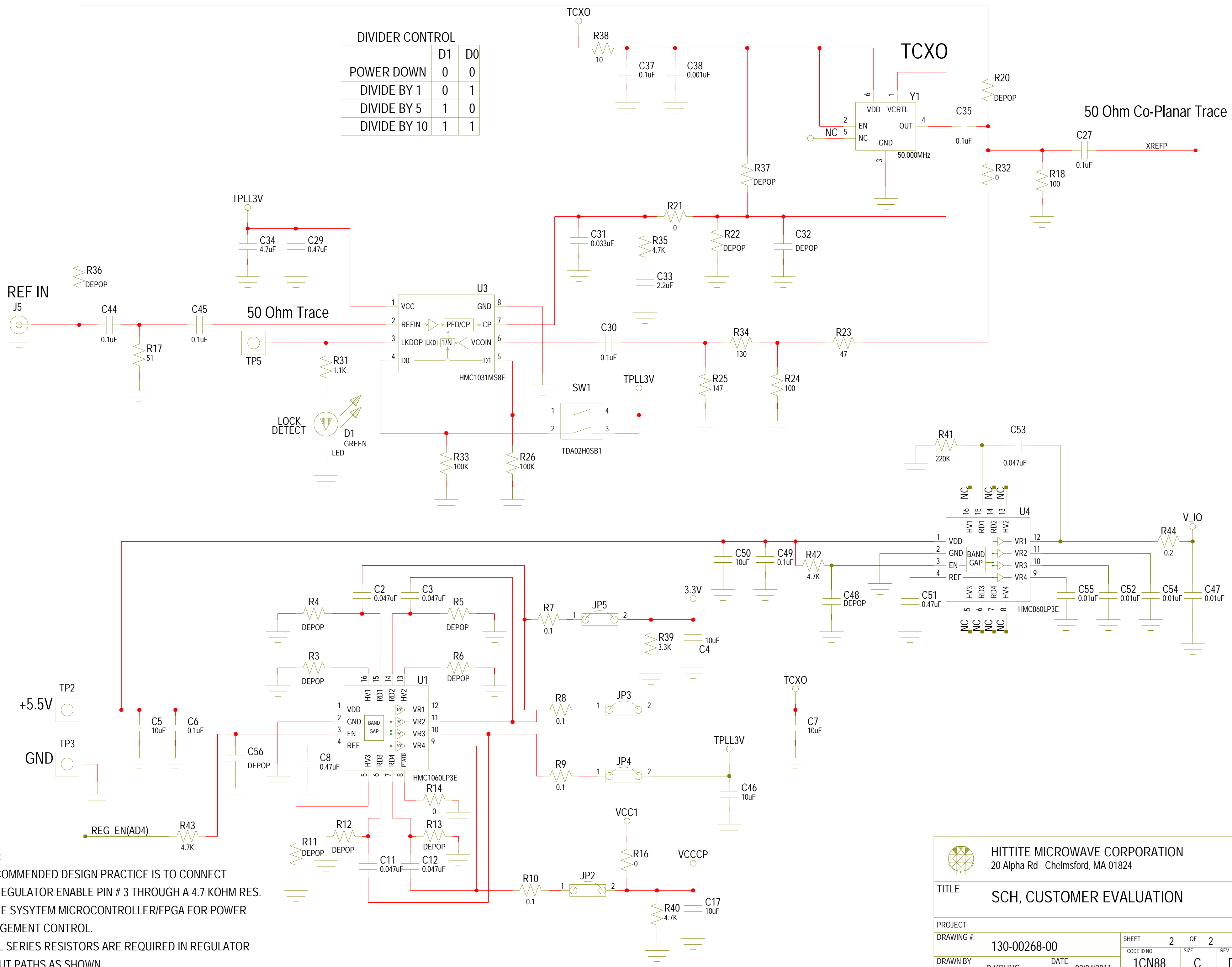


REVISIONS					
REV	ECN#	ZONE	DESCRIPTION	NAME	DATE
C	CP120346	----	CHANGE AS PER CP 120346	D. ACEVAL	04/09/2012
D	CP121059	----	CHANGE AS PER CP 121059	V. VADUVA	10/04/2012

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TITLE SCH, CUSTOMER EVALUATION				
PROJECT DRAWING #: 130-00268-00		SHEET 1 OF 2 CODE ID NO. 1CN88 SIZE C REV D		
DRAWN BY D.YOUNG DATE 02/04/2011				



DIVIDER CONTROL

	D1	D0
POWER DOWN	0	0
DIVIDE BY 1	0	1
DIVIDE BY 5	1	0
DIVIDE BY 10	1	1

NOTE:
 A RECOMMENDED DESIGN PRACTICE IS TO CONNECT THE REGULATOR ENABLE PIN # 3 THROUGH A 4.7 KOHM RES. TO THE SYSYTEM MICROCONTROLLER/FPGA FOR POWER MANAGEMENT CONTROL.
 SMALL SERIES RESISTORS ARE REQUIRED IN REGULATOR OUTPUT PATHS AS SHOWN

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TITLE: **SCH, CUSTOMER EVALUATION**

PROJECT: _____
 DRAWING #: **130-00268-00** SHEET **2** OF **2**
 CODE ID NO. **1CN88** SIZE **C** REV **D**

DRAWN BY: **D.YOUNG** DATE: **02/04/2011**